Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A method for accessing image data in a computer system, said computer system comprising a core logic unit, a system memory having an AGP memory block and a non-AGP memory block, a graphics accelerator, and an image data outputting device in communication with a south bridge chip of said core logic unit, said method comprising steps of:

receiving image data from said image data outputting device by said core logic unit;

writing said image data directly into ~~an~~ said AGP memory block of said system memory instead of said non-AGP memory block; and

accessing said image data in said AGP memory block by said graphics accelerator.

2. (Original) The method according to claim 1 wherein said image data outputting device is a digital still camera or an optical disc drive.

3. (Original) The method according to claim 1 wherein said image data from said image data outputting device are received by a south bridge chip of said core logic unit.

4. (Original) The method according to claim 3 wherein said image data outputting device is electrically connected to said south bridge chip of said core logic unit via an interface selected from a group consisting of USB, IDE, IEEE1934, PCI and LAN interfaces.

5. (Original) The method according to claim 1 wherein said image data in said AGP memory block of said system memory is accessed by said graphics accelerator as a texture.

6. (Original) The method according to claim 1 wherein said AGP memory block of said system memory is in communication with a north bridge chip of said core logic unit via an AGP protocol.

7. (Original) The method according to claim 1 wherein said graphics accelerator is electrically connected to said north bridge chip of said core logic unit via a PCI or an AGP bus.

8. (Original) The method according to claim 1 wherein said step of writing said image data into said AGP memory block of said system memory is performed in a direct memory access mode.

9. (Currently Amended) A method for accessing image data in a computer system, said computer system comprising a core logic unit, a system memory, a graphics accelerator, and an image data outputting device in communication with a south bridge chip of said core logic unit, said method comprising steps of:

receiving image data from said image data outputting device by said core logic unit;

writing said image data into a specified memory block of said system memory, which is accessible by said graphics accelerator, without transference of said image data inside said system memory; and

accessing said image data of said specified memory block by said graphics accelerator.

10. (Original) The method according to claim 9 wherein said specified memory block is an AGP memory included in a system memory.

11. (Currently Amended) A method for accessing image data in a computer system, said computer system comprising a core logic unit, a system memory and a graphics accelerator, said method comprising steps of:

receiving data by said core logic unit;

checking whether said received data is image data;

writing said received data into a specified memory block of said system memory without transference of said received data inside said system memory when said received data is image data; and

accessing said received data in said specified memory block by said graphics accelerator.

12. (Original) The method according to claim 11 wherein said data receiving and checking steps are performed by a south bridge chip of said core logic unit.

13. (Original) The method according to claim 11 wherein said specified memory block of said system memory is a texture memory.

14. (Original) The method according to claim 11 wherein said specified memory block of said system memory is an AGP memory.

15. (Original) The method according to claim 14 wherein said specified memory block of said system memory is in communication with a north bridge chip of said core logic unit via an AGP protocol.

16. (Original) The method according to claim 15 wherein said graphics accelerator is electrically connected to said north bridge chip of said core logic unit via a PCI or an AGP bus.

17. (Original) The method according to claim 11 wherein said step of writing said received data into said specified memory block of said system memory is performed in a direct memory access mode.